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10/634,001	08/04/2003	Ming-Ching Chang	67,200-1107	5032

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EXAMINER	
GEORGE, PATRICIA ANN	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 09/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/634,001	CHANG ET AL.	
	Examiner	Art Unit	
	Patricia A. George	1765	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 03 August 2006.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-23 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Previous final withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 2, 4-9, 11-12, 14-19, and 21-22 rejected under 35 U.S.C. 103(a) as being unpatentable over Lee of USPN 5,665,203 in view of Nallan et al. in 6,902,681 and Grimbergen et al. (6,081,334).

As for independent claims 1 and 14, Lee et al. discloses a method of Reactive Ion Etching (RIE) of polysilicon gate structures for vertical sidewalls (col. 1, l. 6-7) that obtains accurate pattern transfer (col.6, l.39-40). Lee teaches a gate dielectric (fig. 4, 22 and col.3, l.35) formed over a silicon substrate (fig. 4, 21 or col.3, l.32) and a

polysilicon layer (fig.4, 23 and col.3, l.36) formed over the gate dielectric; providing a hardmask layer (fig.4, 52 and col.4, l.11-12) over the polysilicon layer; using a photo resist layer (col.3, l.50) to pattern the hardmask layer for forming parallel N and P type polysilicon gates (fig.5, 12 &13) written on gate electrodes. Lee discloses a method of RIE that has three steps (col.4, l.28) and a typical over etch (col.4, l.57). Lee discloses the first RIE step etches through any oxide that is formed on the polysilicon layer (col.4, l.32-32), written on etching on hardmask layer to expose the polysilicon layer. Lee discloses the second RIE step etches through all but 20 nm of polysilicon which is written on to etch through a first thickness portion of the polysilicon layer. Lee discloses a third RIE step that has a polysilicon to silicon oxide selectivity (col.4, l.52), which is written on etching through the second thickness portion of the polysilicon layer. Lee also discloses the bias power is at 50 watts (col.4, l.54), a lower setting than use for the second RIE step, 200 watts (col.4, l.41) (as in claims 5 and 15). Lee discloses a third RIE step that is timed to reach the gate oxide (col.4, l.59), then carrying out an RIE overetch process to remove the remaining thickness of the polysilicon layer.

Lee does not disclose plasma treating the exposed gate dielectric and polysilicon layer in-situ wherein the plasma is formed essentially from an inert source gas to neutralize an electrical charge imbalance, as in claims 1 and 14.

Nallan et al. teaches plasma treating the gate dielectric, a high-k material (col.2, line 20-35), as in claim 11 and 21, and polysilicon layer in-situ (col. 2, lines 52-53), where the plasma is formed essentially of an inert gas source (col.5, line 2 shows ranges for gas including the option of 20 sccm Cl2, 2 sccm CO, and 200 sccm N2) (as

in claims 6, and 16). Nallan et al. teaches the bias power may be pulsed at 0 and 300 watts (col. 3, l. 60-64), which illustrates zero RF bias as in claim 2.

Nallan et al. does not implicitly teach the treatment would "neutralize the electrical charge imbalance" as in claims 1 and 14. Nallan's treatment provides the process conditions claimed by applicants, therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made, that Nallan's plasma treatment formed essentially of an inert gas source would have the same function as applicants' claimed invention "neutralize the electrical charge imbalance" because Nallan's plasma treatment provides the same process conditions claimed by applicant.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include a plasma treatment step to the exposed gate dielectric and polysilicon layer in-situ wherein the plasma is formed essentially from an inert gas source to neutralize the electrical charge imbalance, as in applicants claims 1 and 14, when etching a polysilicon gate profile, as Schoenborn, because Nallan et al. teaches it is a process improvement which protects the polysilicon electrode and underlying silicon, avoiding making transistors defective or inoperable (see col.1, l.35-48), which would impart added benefits of fewer electrical defects, a higher yield, and cost savings.

The modified reference of Lee is silent as to the use of endpoint detection, when etching the polysilicon, to expose the gate dielectric, as in claims 1, and 14.

Grimbergen et al. teaches the well known technique of etching to endpoint detection particularily for thin layers, such as gate dielectrics, to prevent damage to

them when etching polysilicon or silicon. Grimbergen et al. teaches as the gate dielectric becomes thinner and thinner, in high speed integrated circuits, it becomes more difficult to accurately etch through the overlying polysilicon layer without overetching into the gate oxide layer, particularly when halogen and fluorine containing gases (that etch through polysilicon with high etch rates) are used. Grimbergen et al. teaches end point detection is desirable because it prevents charge damage and lattice structural damage upon exposure to the energetic plasma ions (see Background).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include the use of endpoint detection, as Grimbergen et al., when etching polysilicon to expose the underlying gate dielectric, as the midified invention of Lee, because Grimbergen et al. teaches the method is well known to prevent charge damage, a process improvement which decreases defect density, and increases yield.

As for claim 4, Lee illustrates in figure 2 (parts 28 and 30) that the polysilicon layer includes both n and p doped regions used to form doped polysilicon gate electrodes shown in parallel (col.3, l.42-46).

As for claims 7-8 and 17-18, Lee discloses the third and fourth RIEs are carried out with 45 sccm of HBr, 3 sccm (70%) of He, and 30% O2, which as claimed, is a chlorine-free etching chemistry comprising HBr and oxygen.

As for claims 9 and 19, Lee discloses a combination of HBr/Cl.sub.2/O.sub.2 in the first and second etch steps (col.4, l.39-40 and c.4, l.46-50).

As for claims 11 and 21, Lee discloses the gate dielectric is thermally grown SiO.sub.2 (col.3, l.33-34). .

As for claims 12 and 22, Lee discloses the hardmask layer is LTO (col.3, l53 and 55).

As for claims 5 and 15, Lee is silent on the topic of RF source power and does not reference it, including the lowering the source power in the third step.

Claim Rejections - 35 USC § 103

Claims 3, 10, 13, 20, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee and Nallan et al., as applied to claims 1, 2, 4-9, 11-12, 14-19, and 21-22 above, further in view of Lill et al. of USPN 6,284,665.

The combined invention of Lee teaches the benefits of self-bias and the benefit of reducing etching bias with an over etch step, but never discloses the RF bias is set to zero. Lee is also completely silent about RF frequency, or that it is adjustably decoupled.

Lill et al. teaches typical process conditions for RIE of polysilicon selectively to silicon nitride. Lill teaches the use of no-bias power to minimize the amount of self-bias on the substrate (col.10, l.15-30), as in claims 3, 13, and 23. Lill also teaches the RF bias power is supplied at the claimed frequency of greater than about 1 MHz (col.8, l.4) and in figure 2 Lill illustrates the RF bias power and is adjustably decoupled (col.10, l.4) from the RF source power, as in claims 10 and 20.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to use the typical process conditions for RIE of polysilicon selectively to silicon nitride, of Lill, when using the method of RIE for polysilicon gate structures, of Lee, because Lill teaches they are typical for RIE of polysilicon.

Claim Rejections - 35 USC § 103

Claims 1 – 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schoenborn in US 5,242,536 in view of Lee et al. in US 5,665,203 and Kim et al. in US 6,620,575 and Winniczek et al. in US 6,093,332, Nallan et al. in 6,902,681 and Grimbergen et al. (6,081,334).

Schoenborn discloses an improved method for controlling (i.e. improving) the profile of a polysilicon gate electrode in a polysilicon etch process (see section on invention background). Schoenborn discloses a method to etch a polysilicon profile (i.e. electrode) (col.3, lines 7-8), formed over an oxide gate (i.e. dielectric layer) (see abstract) formed over the substrate, a monocrystalline silicon wafer (col.3, lines 21-23). Schoenborn discloses it is common to place a resist material over the silicon layer (col.2, lines13-15) and goes on to include oxide (which illustrates silicon oxide as in claim 12 and 22) a well known material used to obtained verticles profiles (i.e. hard mask) (col.1, lines 40-43 and col.2, l.24-26). Schoenborn discloses plasma etch (i.e. RIE) process are well known, and starts by discussing a beginning process (i.e. first step) to form masking patterns that are used to protect the areas of the wafer from the etch process, which illustrates a thickness of the mask layer has been removed to

expose the polysilicon which will be etched to form a polysilicon gate electrode. Next, the second step, Schoenborn discloses is a silicon etch which uses minimal etching bias and low power for bulk polysilicon removal (col. 1-2, lines 38-2). And finally, a third step, a limited overetch cycle which selectively etches the poly to oxide which discloses a selectivity of poly:oxide, illustrating etching through a second thickness portion of the polysilicon layer to expose portions of the under lying gate dielectric (col.4, lines 3-7). Schoenborn discloses Etching chemistry of HBr/Cl2 and the presence of O2 unavoidable, either through the intentional addition of O2 or the presence in the chamber from leaks.

Schoenborn discloses doped polysilicon regions (col.2, 30-31), as in claim 14, but is silent as to how or what they are doped with, such as n-doped and p-doped, as in claim 14.

Lee et al., in US 5,665,203, discloses it is well known that a function of the polysilicon layer is to have both n and p type doped regions that form separate electrodes, as in claims 4 and 14 (see col.3, lines 59-67).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include the doped regions of the polysilicon layer, of Schoenborn, are n-doped and p-doped, as in Lee, because Lee illustrates (see fig. 1-5) it is well known and functional for polysilicon to be doped.

Schoenborn does not teach the third and fourth RIE process steps are carried out with HBr and O2, (chlorine free) as applicants limitations of claims 7, 8, 17, and 18.

Lee et al. also teaches the RIEs process step are carried out with 45 sccm of HBr, 3 sccm (70%) of He, and 30% O2, which as claimed, is a chlorine-free etching chemistry comprising HBr and oxygen, as in claims 7, 8, 17, 18, and 19.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to use the chlorine free chemistry, of Lee, when etching the third and fourth process RIE step, as in applicants' claims 7, 8, 17, 18, and 19, because Lee teaches it is effective.

Schoenborn discloses systems to use for polysilicon etching, which are commonly known to be configured for rf source and bias power. However Schoenborn is silent about rf source and bias power in the second step, as in claim 14 (See col.2, lines 47-55.) and that the bias power is about 1 Mhz adjustably decoupled from the rf source, as in claim 10 and 20.

Kim et al. in US 6,620,575 teaches polysilicon etch with rf power at both source and bias (see Table 1) and that the bias power is 1 Mhz adjustably decoupled from the rf source (col.7, l. 5-15), as in claim 10 and 20.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include rf source and bias power, as Kim, when etching polysilicon in a system that is configured for rf source and bias power, as Schoenborn, for applicants' second etch step, because Kim teaches (see Figure 9) that CD bias is a function of plasma source and bias power and directly relates to the CD of the patterned masking material of built up structures which achieves advantageous physical

bombardment of the surfaces contacted by the plasma, helpful to apply a bias to the patterned mask and underlying substrate.

Schoenborn does not disclose using lower etch power in the third step than in the second RIE step, the lower power selected from the group consisting of 1) a lower RF source power, 2) a lower RF bias power, as in claims 1, 5, and 14 and Schoenborn is silent about zero rf bias in the overetch process which removes remaining portions of polysilicon., as in claims, 3, 13, 14, 15, and 23.

Winniczek et al. in US 6,093,332 teaches pulsing an RF power source at a predefined frequency to provide pulsed RF power to the chuck (see summary of invention), which illustrates zero rf power, while etching any masked material, to include polysilicon (col.3, line 47). Winniczek et al. teaches this masked pattern etch method has the benefit of reducing erosion of the mask due to polymer deposition on the mask, as in claims 3, 13, 14, 15, and 23.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to use the process of pulsed power, providing zero rf power to the chuck, as in Winniczek et al., when performing applicants' third and overetch step, because Winniczel teaches a benefit of reducing mask erosion through polymer deposition.

Schoenborn is silent as to plasma treating the exposed gate dielectric and polysilicon layer in-situ wherein the plasma is formed essentially from an inert gas

source to neutralize the electrical charge imbalance, as in claims 1, 2, 6, 14, and 16; and the type of oxide the gate dielectric is, such as high-K as in claim 11 and 21.

Nallan et al. in 6,902,681 teaches plasma treating the gate dielectric, a high-k material (col.2, line 20-35), as in claim 11 and 21, and polysilicon layer in-situ (col. 2, lines 52-53), where the plasma is formed essentially of an inert gas source (col.5, line 2 shows ranges for gas including the option of 20 sccm Cl2, 2 sccm CO, and 200 sccm N2) (as in claims 6, and 16). Nallan et al. teaches the bias power may be pulsed at 0 and 300 watts (col. 3, l. 60-64), which illustrates zero RF bias as in claim 2.

Nallan et al. does not teach the treatment would "neutralize the electrical charge imbalance" as in claims 1 and 14. Nallan's treatment provides the process conditions claimed by applicants, therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made, that Nallan's plasma treatment formed essentially of an inert gas source would have the same function as applicants' claimed invention "neutralize the electrical charge imbalance" because Nallan's plasma treatment provides the same process conditions claimed by applicant.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include a plasma treatment step to the exposed gate dielectric and polysilicon layer in-situ wherein the plasma is formed essentially from an inert gas source to neutralize the electrical charge imbalance, as in applicants claims 1 and 14, when etching a polysilicon gate profile, as Schoenborn, because Nallan et al. teaches it is a process improvement because which protects the polysilicon electrode and

underlying silicon, avoiding making transistors defective or inoperable (see col.1, l.35-48).

The modified reference of Lee is silent as to the use of endpoint detection, when etching the polysilicon, to expose the gate dielectric, as in claims 1 and 14.

Grimbergen et al. teaches the well known technique of etching to endpoint detection particularily for thin layers, such as gate dielectrics, to prevent damage to them when etching polysilicon or silicon. Grimbergen et al. teaches as the gate dielectric becomes thinner and thinner, in high speed integrated circuits, it becomes more difficult to accurately etch through the overlying polysilicon layer without overetching into the gate oxide layer, particularly when halogen and fluorine containing gases (that etch through polysilicon with high etch rates) are used. Grimbergen et al. teaches end point detection is desirable because it prevents charge damage and lattice structural damage upon exposure to the energetic plasma ions (see Background).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include the use of endpoint detection, as Grimbergen et al., when etching polysilicon to expose the underlying gate dielectric, as the midified invention of Lee, because Grimbergen et al. teaches the method is well known to prevent charge damage, a process improvement which decreases defect density, and increases yield.

Response to Arguments

As to applicants' argument on page 16, Lee clearly teaches a third step of RIE, then an RIE overetch process, see reference above.

Applicants' argue, on page 16, that Lee does not disclose a plasma treatment following endpoint detection and exposure of underlying gate dielectric.

The reference of Lee teaches plasma treatment (see discussion above) and exposing the gate dielectric (fig.4, part 22), but not endpoint detection, as this is a newly amended limitation.

Applicants' argue that Nallan does not disclose a process for etching a gate electrode, although applicants' aknowledge the process of Nallan discloses it follows a step of etching a gate electrode.

Applicants' agrue on pages 17-18 that there is no motivation to combine the teachings of Nallan and Lee. Examiner relies on the reference of Nallan for the teaching plasma treatment of the gate dielectric. Nallan teaches benefits, cited above, for such a treatment. Examiner finds said benefits to be motivation to combine the two references. Both references are related to the forming of a functional gate. Nallan makes improvements in the art, to the function of the gate.

Applicant's argue, on page 18, that modifying the process of Lee with the process of Nallan would make the process of Lee unsuitable because of a subsequent step that makes it inconsistent with an oxygen cleaning plasma process. Examiner disagree, as the reference of Lee was used to teach RIE steps, and believes Lee's step of Hf cleaning may be benifitial at any stage of fabrication.

As to applicants' argument on page 19, that prior art of the action filed, 4/11/2006, not teach the newly amended limitation, examiner agrees. Please see new rejection above.

Applicant's asserts, on page 20, that the process of Nallan is a high-K gate dielectric etching process, yet examiner relies on the reference of Nallan solely for the teaching of treatment of the gate dielectric.

Applicants assert, on page 22, that one of ordinary skill would not interpret pulsed RF power to be equivalent to Applicants' claim, in light of a statement in the specification "plasma treating is carried out using zero bias power". Examiner disagree, as Nallan clearly teaches rf power at zero. Applicants' do not cite negative limitations in the claims to exclude the use of pulsed rf power.

Once again, on page 23, applicants' assert the newly amended limitation is not addressed in the references used to overcome the claims previously presented.
Also on page 23, applicants address that none of the references disclose applicants' effect, to neutralize an electrical charge imbalance. Examiner addressed this limitation, on page 4, of the prior action, and exerts that it would be obvious for the same functions to occur from a process which provides the same process conditions.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patricia A. George whose telephone number is (571)272-5955. The examiner can normally be reached on weekdays between 7:00am and 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571)272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Patricia A George
Examiner
Art Unit 1765

PAG
08/06

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